Handling Faults in CANopen and EtherCAT

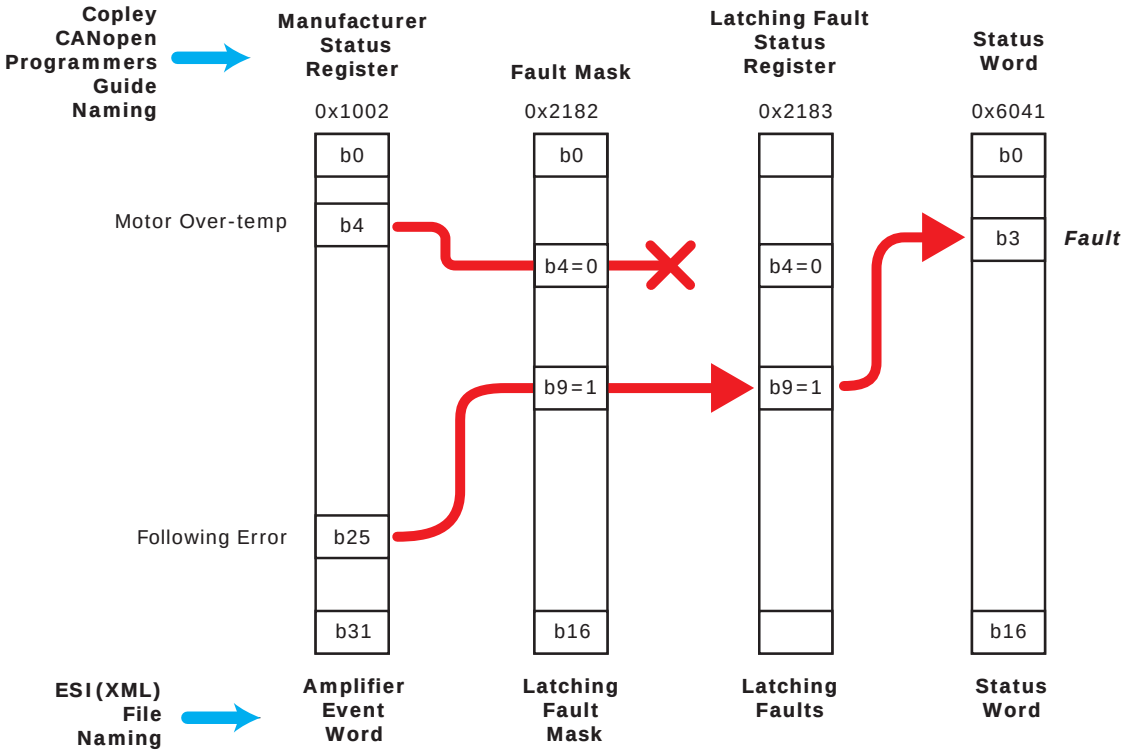
ABOUT FAULTS

- The *Manufacturer Status Register* (0x1002) is a real-time monitor of conditions in the drive
- Some of these conditions are linked to the *Latching Fault Status Register* (0x2183) Whenever this 16-bit register does not equal zero, a *Latching Fault* occurs
- The *Fault Mask* (0x2182) determines which ESR bits are allowed to pass into 0x2183 Bits must be set (1) for ESR bits to pass into 0x2183 and produce a *Latching Fault.* A bit that is zero will prevent an ESR condition from producing a *Latching Fault*
- *Latching Faults* force the drive to disable and set bit 3 of the *Status Word*

FAULTS HAPPEN

Suppose that the motor is over-heating and as a result a follow error occurs. The graphic below shows how this might be handled.

- Bits 4 and 25 in the *Amplifier Event Word* are set
- The *Fault Mask* has a 0 in bit 4 so that the motor condition doesn't generate a latching fault. Bit 9 is a 1 because an excessive following error should shut the drive down to protect the equipment.
- Bit 9 in the *Latching Faults* object goes to 1 and a latching fault occurs
- The *Status Word* shows the fault when bit 3 is set. This is the "check engine" indicator that demands action to deal with the fault.



CLEARING FAULTS

- First, *ELIMINATE THE CAUSE OF THE FAULT !!*
- Next, clear the *Latching Fault* register
  Write 1's into the associated bit of each fault to be cleared.
  To clear the entire 32-bits, write 0xFFFFFFFF to 0x2183
- Clear the *Latched Event Status Register* 0x2181
  This is like a memory of all the momentary Amp Events and will contain the events that produced the latching fault. Clear this the same way as the 0x2183
  by writing 1's bit-by-bit, or 0xFFFFFFFF to clear them all.
- Clear the *Sticky Event Status Register* 0x2180
  Like 0x2181, this is a memory-register of Amp Events, but is cleared
  simply by reading it.
- When *Latching Faults* has been cleared and no fault conditions exist in the drive,
  Status Word bit 3 will clear and the drive can be re-enabled.

CLEARING FAULTS IN CME2

- First, CME2 clears the *Latching Fault* register by writing 0xFFFFFFFF to it.
- Byte 1 of the string is the node address, typically 00 when not multi-dropped
  Byte 2 is a checksum
  Byte 3 is the number of 16-bit word that follow the first four bytes (the header)
  Byte 4 is the op-code: 0d (13) writes to a parameter to set a value
  Bytes 5~6 is the first word (msb first), and specifies parameter 0xa4 (0x2183)
  Bytes 7~8 are the second word, data, and is 0xFFFF (the upper 16-bits)
  Bytes 9~10 are the third word = 0xFFFF (the lower 16-bits)
  The parameter is a 32-bit value so two 16-bit words are needed to send the data
- Repeat this process for parameter 0xa1 (0x2181)