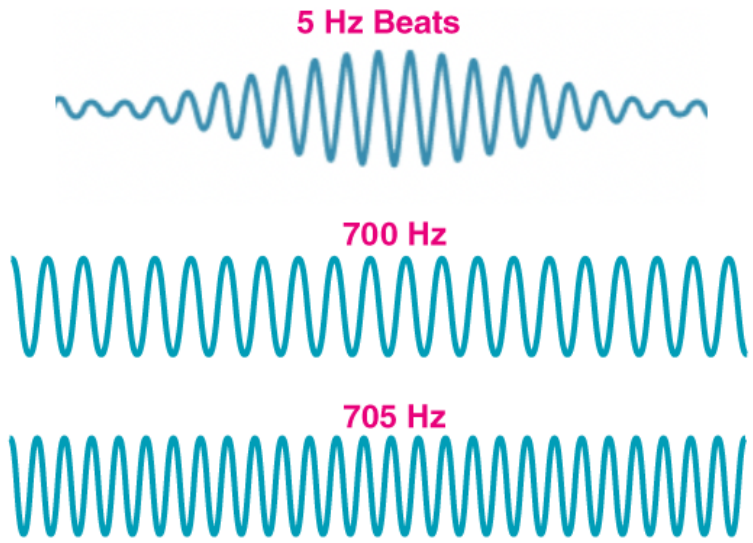
Introduction

CANopen and EtherCAT master controllers perform clock synchronization across a network by configuring a slave drive to transmit a high-resolution sync or time stamp. The clock on a slave drive is typically more accurate than a clock on a PC. This will ensure that there are no time misalignments between the master and the slave nodes and among the drives themselves. However, some systems do not have an advanced master controller or have a type of master controller with no sync control. As the PWM output of a drive is synchronized with the drive clock, one potential problem of clock drift between unsynchronized drives is the possibility of a beat frequency visible on drive current sensors due to cross talk related to poor cabling, grounding, and shielding.

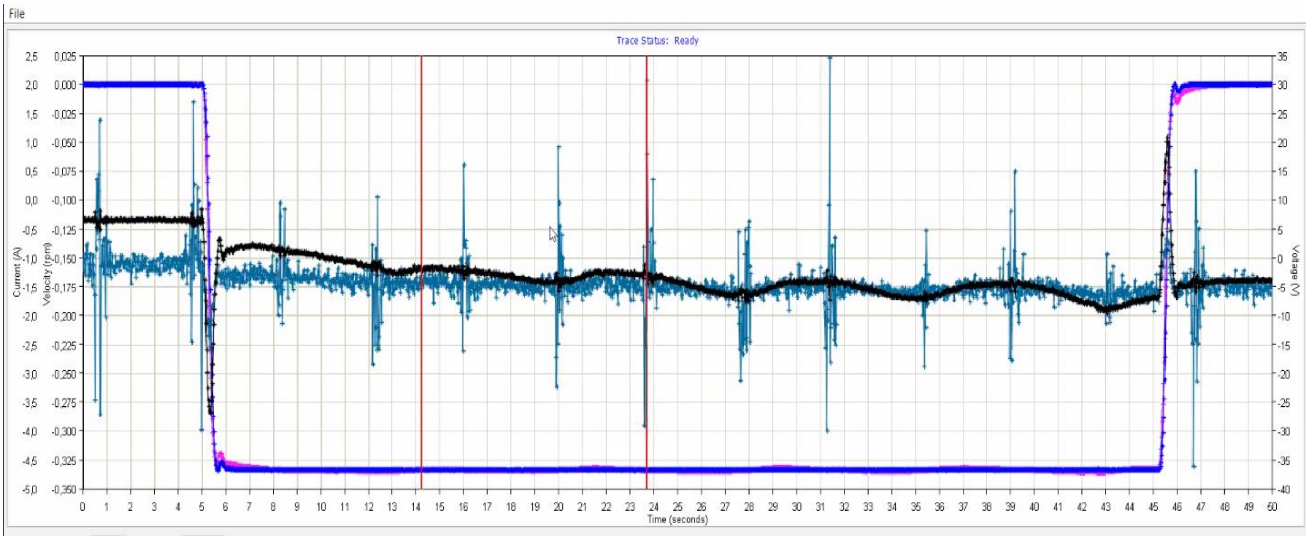
Beat Frequency

A beat frequency occurs as a result of two unsynchronized frequency signals. The resulting beat is caused by the constructive and destructive interference between the two frequencies, as shown in the image below. Given by $f_b = |f2–f1|$



When using a PWM output of a servo drive, switching typically at 16k khz, a beat frequency can occur if the drive's clocks are not synchronized. As mentioned before when using a CANOpen or EtherCAT master the system's timing is controlled by the protocol due to a SYNC message. More information on network synchronization can be found in AN100 - EtherCAT Synchronization

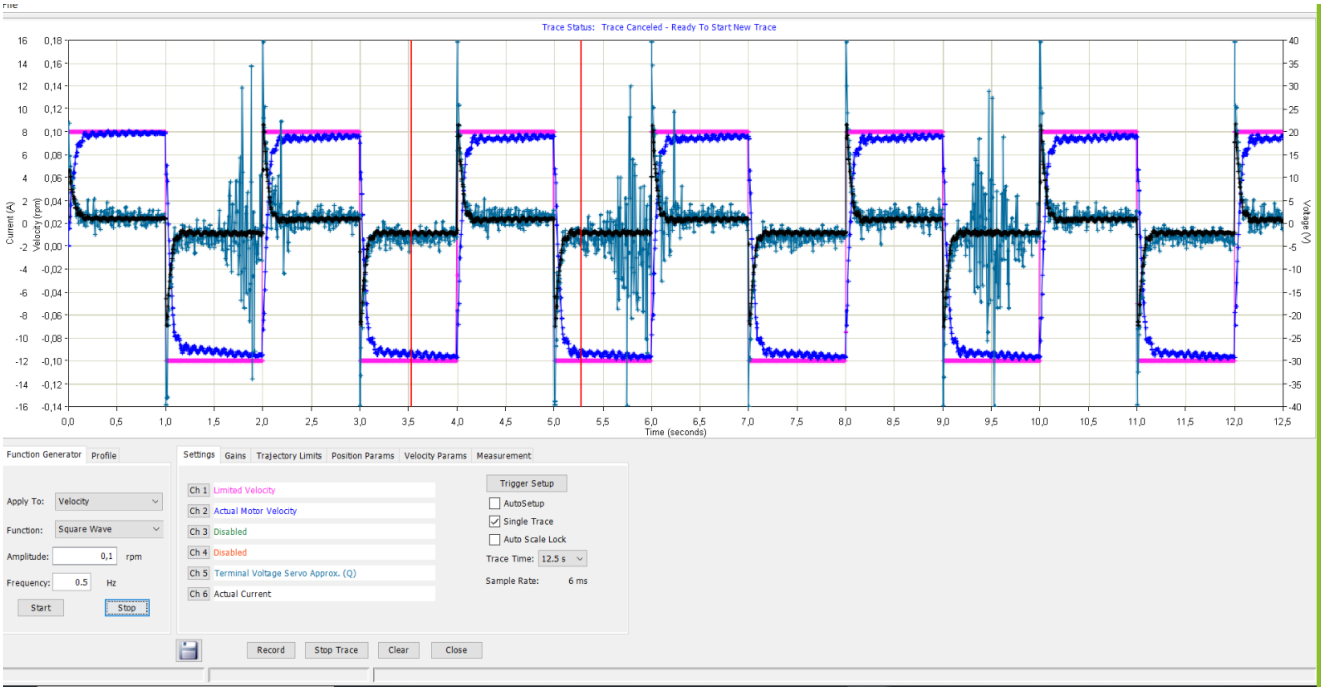
When such a protocol is not used Copley's PWM SYNC OUT/IN can be used if the beat frequency is present. A beat frequency can look like a waveform, and the image below displays a beat frequency of every 4 seconds. In some applications it is possible the beat frequency causes the mechanics to resonate and make a sound similar to the sound of a very tight motor tuning.



Before using the PWM Sync option, double-check and make sure the motor has a good solid path to earth. If a beat frequency is seen every few seconds in the current or position loop then we should suspect clock drift between drives and poor cabling, grounding, and shielding in the system. When a motor has a poor path to earth, PWM switching edges will couple from the motor coil to the motor case through the Miller capacitance effect. This noise could also flow to other poorly shielded cables like another motor's power cable and be picked up by the drive's current sensors during the otherwise "quiet" time when current is measured. The solution to the beat frequency is to make sure motor case have a good solid path to earth and that motor cables have a good P-clamping path to earth at the drive.

How to connect

To properly connect the PWM SYNC output to the drive's input(s), one must consider that the inputs need to be of type HS (high-speed) and the outputs need to be GP (General speed), or HS (high-speed) outputs (with respect to ground). Refer to the corresponding datasheet of your drive to find out which outputs and inputs you need. In the scope trace below, two APV drives are connected to the same power supply with no PWM SYNC connection and are making a move every resulting in a beat frequency every four seconds.



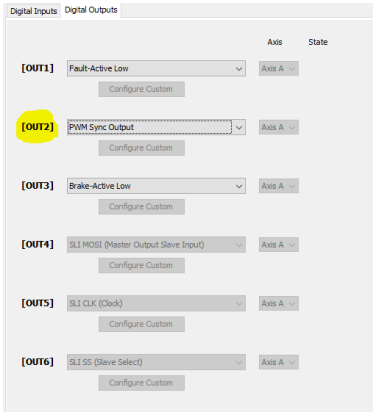
According to the datasheet, output 2 of the APV is a high-speed output and input 2 is a high-speed input. Make sure the ground of one drive is connected to the ground of the other drive. If necessary, use an additional wire to make sure the grounds are connected. Connect the master Output 2 to the slave Input 2. The master will send out a signal that is received as a PWM sync input by the slave. That is if it is configured to do so in CME.

Configuring CME

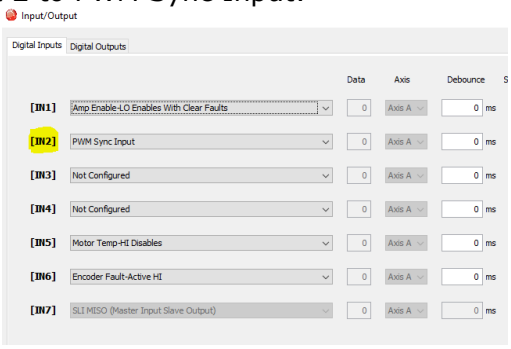
Configuring option 1 (FPGA):

To configure the master drive to send out the PWM sync output and the slave PWM Sync input, all that needs to be done is to set the input and output on the drives using CME respectively.

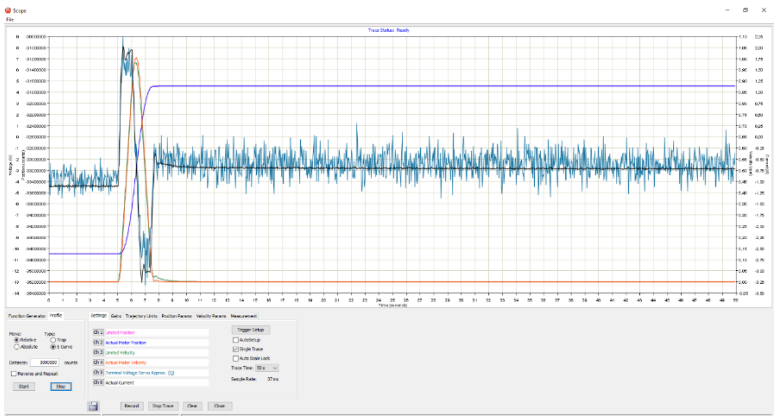
On the master drive, for example in an APV, set output 2 to PWM Sync Output:



On the slave drive set input 2 to PWM Sync Input:

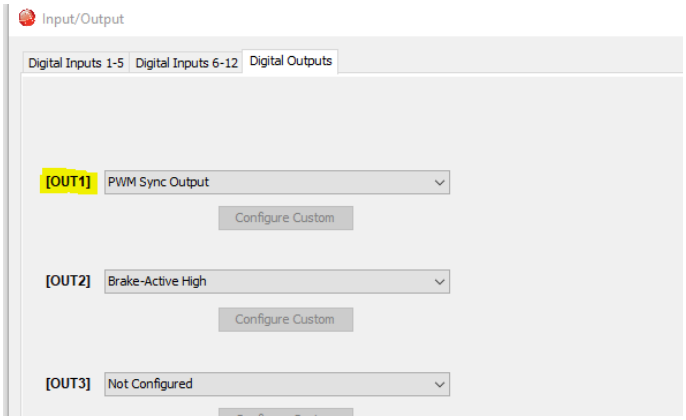


Save both configurations to Flash and run a trace on the scope again. The result should be visible in the scope trace as shown here below. We can use PWM SYNC OUT fanned out to multiple axis PWM SYNC IN to synchronize the clocks and PWM transitions to prevent the beat frequency.

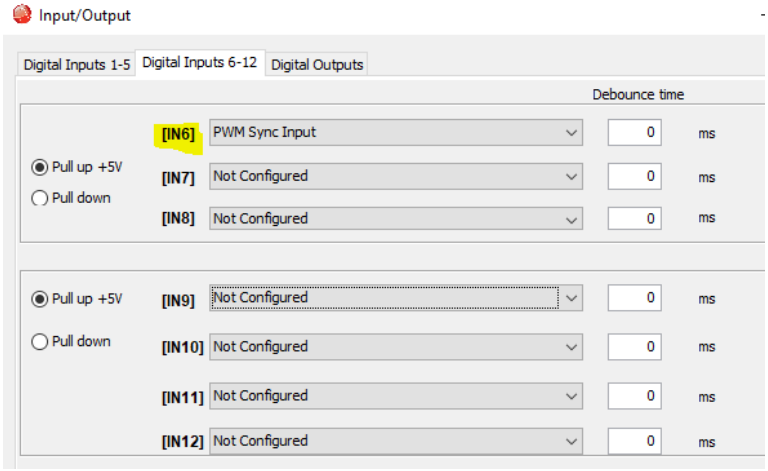


Configuration option 2 (ARM):

To configure a drive with an ARM processor such as the ADP, different I/O need to be selected. For the master ADP select Output 1 as the PWM Sync Output:

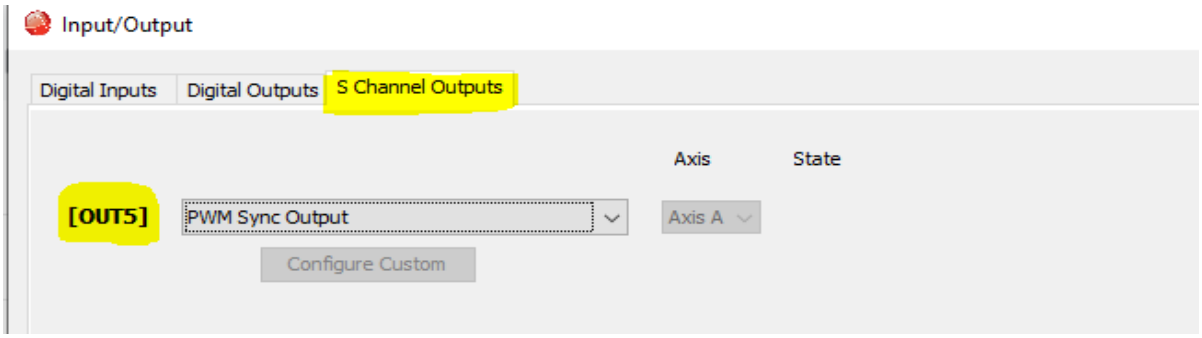


For the slave drive(s) select Input 6 as the PWM Sync input:

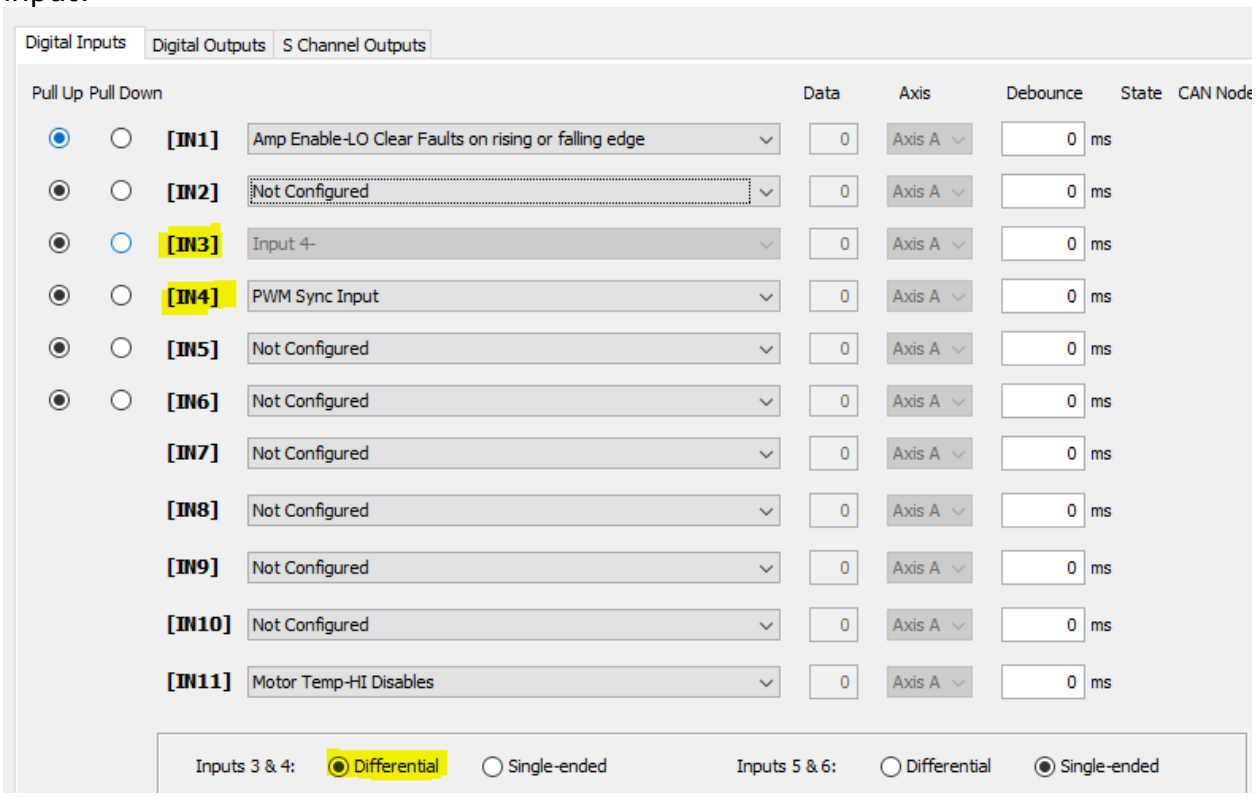


We can use PWM SYNC OUT fanned out to multiple axis PWM SYNC IN to synchronize the clocks and PWM transitions to prevent the beat frequency. Make sure to set the master drive up on your system that has the highest current output range. A 300mA FET output can source 50 5mA sinking inputs.

Configuration option 3 (B*L, T*L drives specific):
The configuration for B*L, T*L drives are different since they are not equipped with a high-speed output by default. To use the PWM Sync feature, the high-speed S-channel is used as an output. To select this option in CME, open the tab **S Channel Output** in the I/O screen:



Because the S-channel is a differential output, the inputs need to be set to differential too. Select the option differential in the Digital Inputs tab and set input 4 to PWM sync input:



Revision History

Date	Version	Revision
5/17/2021	Rev 00	Initial release